



July 1998-2

XRT5897ES

**Demo Board
User Manual**

Overview

This unit is a 7.0 by 7.0 inch circuit board that simplifies the evaluation of the XRT5897 seven channel, 3.3 V, E1, line interface unit integrated circuit. Its features include use of a 4-layer circuit board to minimize noise, provisions for an equipment-side loopback that simplifies testing, and options for operation either with or without an external LOS (Loss of Signal) output delay clock. Figures 1 and 2a through 2e and Table 2 show the demo board component layout, circuit diagram, and parts list respectively.

Power Requirements

A well-regulated source of +3.3 Volts \pm 5%V must be applied to the board at the red (positive) and black (negative) banana jacks.

Equipment-side Digital Input and Output Connections

The component layout given in Figure 1 shows the location of the equipment-side digital receiver input and transmitter output connections for each of the seven independent transmitters and receivers. For versatility, the I/O connections on each channel may be made to either a set of 6 test points, or to a 10-pin header that will accept a ribbon cable connector. The tests points are convenient for lab evaluations and signal monitoring, while the ribbon cable connections offer a method of integrating the XRT5897 board into a larger system.

Table 1 shows the I/O connections for Channel 1. It also applies to the other channels if the digit indicating the Signal and Test Point name is changed to the appropriate channel (e.g. "1" in RXPOS1, etc.). Note the pin 1 locations for the ribbon cable connectors that are shown on the component layout. Pin 1 is at top left for Channels 1, 7 and 6, and at bottom right for Channels 3, 2, 5 and 4. The schematic diagram given in Figure 2 may be used to verify these connections.

Signal Name	Ribbon Cable Connector Pin	Test Point Name
Receiver 1 loss of signal output	1	LOS1
Receiver 1 positive data output	2	RXPOS1
Ground	3	-
Receiver 1 negative data output	4	RXNEG1
Ground	5	-
Transmitter 1 positive data input	6	TXPOS1
Ground	7	-
Transmitter 1 negative data input	8	TXNEG1
Ground	9	-
Transmitter 1 clock input	10	TXCLK1

Table 1. Equipment-side Signal Connections

Note: *Installing the two jumpers next to a ribbon cable connector implements an equipment-side loopback on that channel.*

Transmitter Line Output and Receiver Line Input Connections

Three-circuit one quarter inch audio-type jacks are used for the transmitter line-side output and receiver line-side input of each channel. These jacks accept the patch cord plugs that are commonly used for interconnecting the 120 Ohm balanced lines that are used with E1 test equipment.

Loopback Provisions

A signal source capable of transmitting and receiving dual-rail data having TTL or 3.3 V CMOS compatible levels is necessary in order to test the XRT5897 receivers and transmitters individually. Commercially-available E1 test sets normally do not operate with these signals. However, an equipment-side loopback permits operation of the demo board with readily available test equipment. This loopback may be implemented on any channel by installing the two jumper shunts located next to the 10-pin ribbon cable connector for that channel. If these shunts are installed on Channel 1, the receiver outputs RXPOS1 and RXNEG1 are connected to the transmitter inputs TXPOS1 and TXNEG1 respectively. Now, Channel 1 may be tested by connecting the output of an E1 pattern generator to the Channel 1 receiver input, RX1, and the 120 Ohm input of an error detector to the Channel 1 transmitter output, TX1.

LOS Circuit Operation

The XR-T5897 has a built-in LOS (Loss of Signal) delay that meets the ITU G.775 requirements. Additionally, an external clock may be used to extend this built-in delay. If the pins on the 2-pin header labeled LOS SELECT are open, and nothing is connected to the BNC connector labeled LOS CLOCK, the built-in LOS delay is used. To extend this delay, install the LOS SELECT jumper and apply an external clock to the LOS CLOCK input. Now, the ITU G.775 delay is extended by the period of the externally-supplied LOS CLOCK multiplied by 4096.

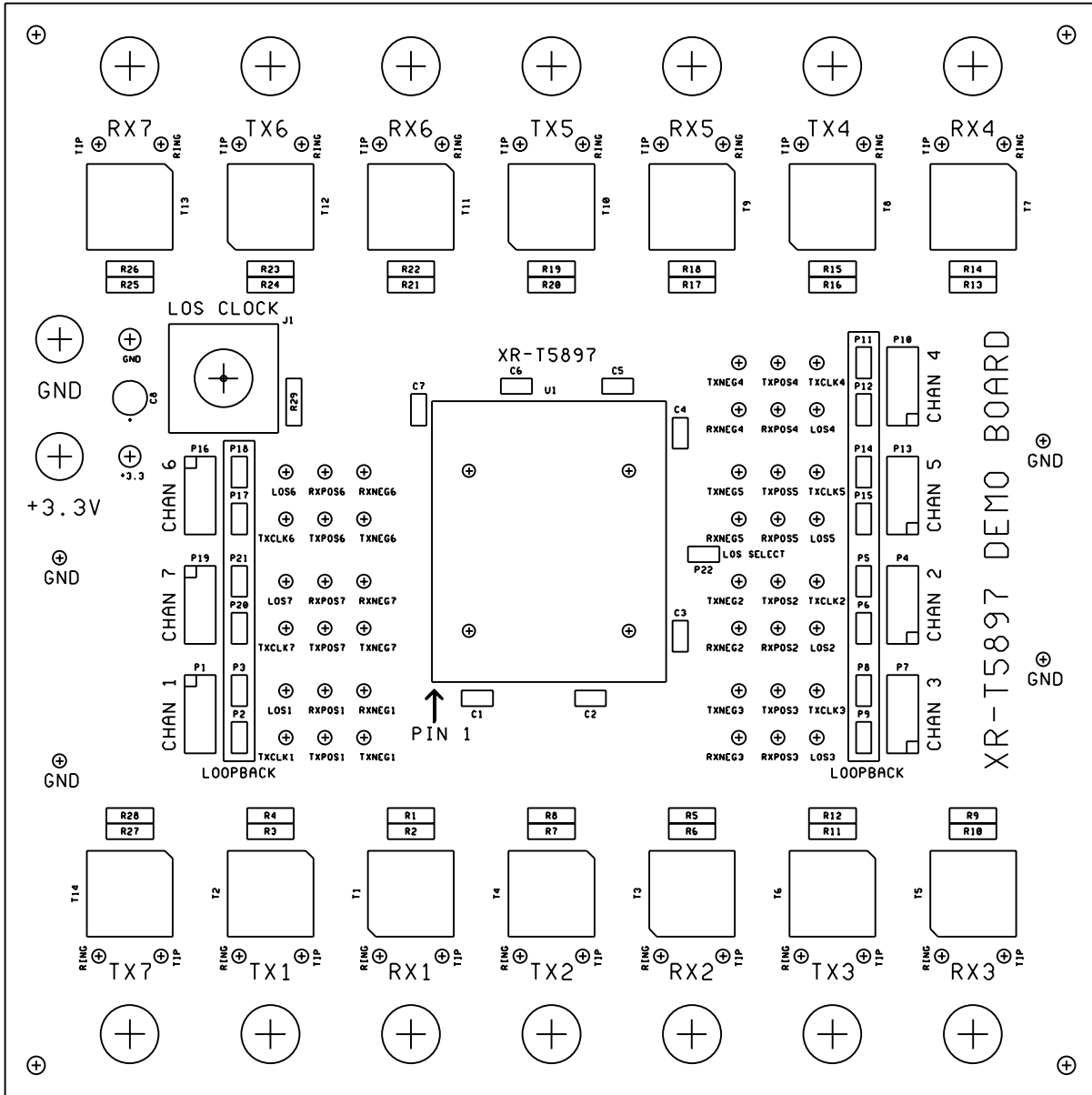
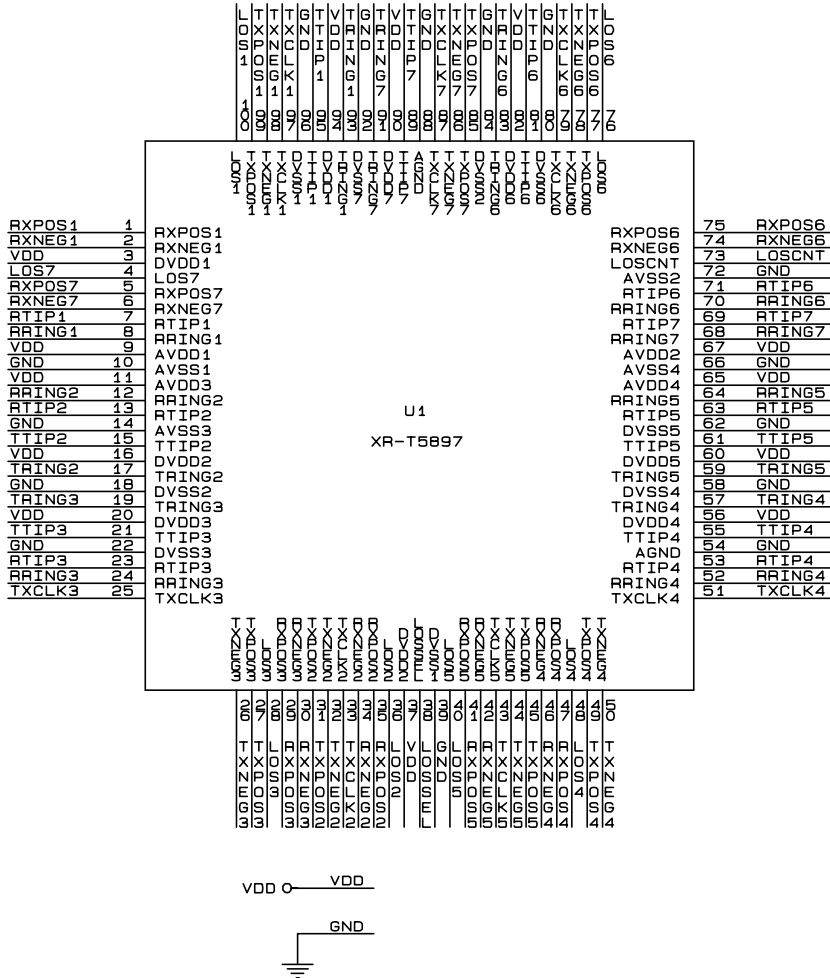
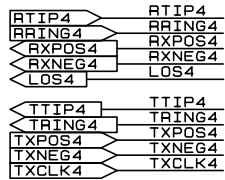
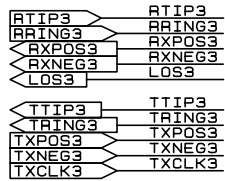
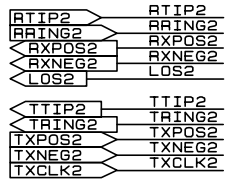
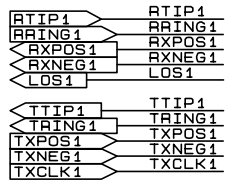


Figure 1. XR-T5897 Demo Board Component Layout



| LINK
| T5897A.SCH
| T5897B.SCH
| T5897C.SCH
| T5897D.SCH

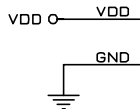
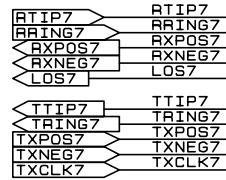
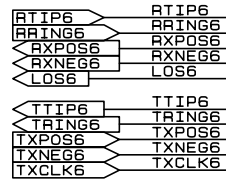
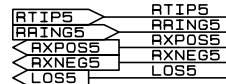
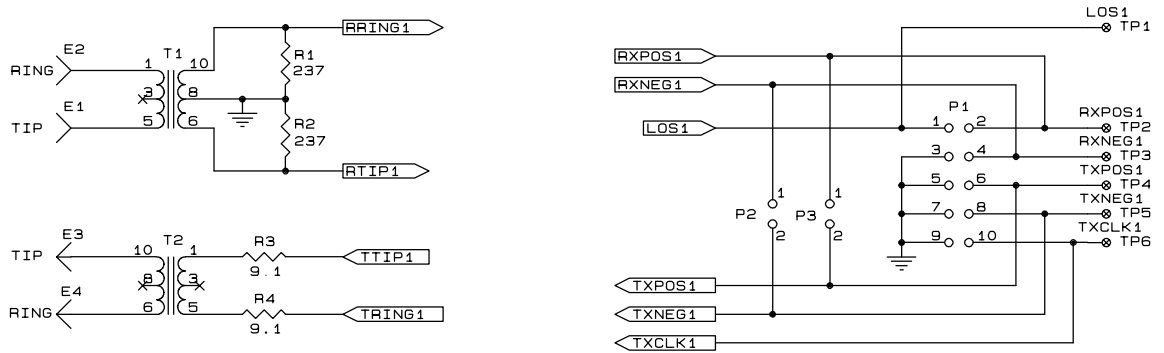
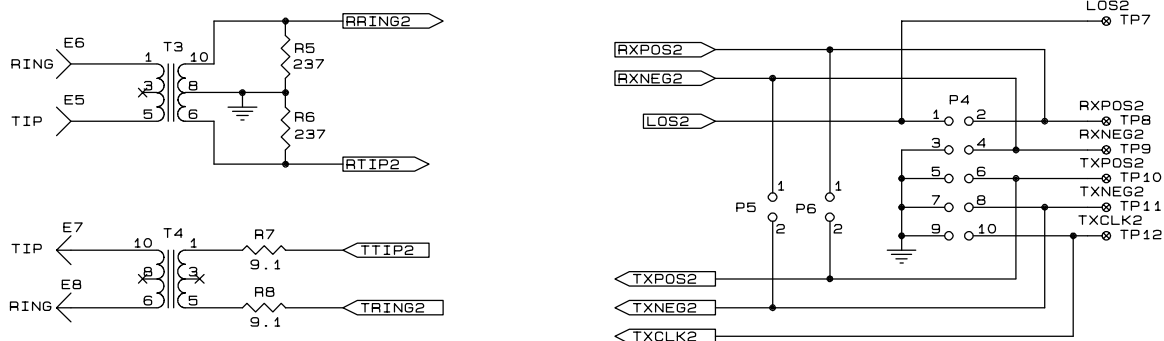


Figure 2a. XRT5897 Demo Board Circuit Diagram

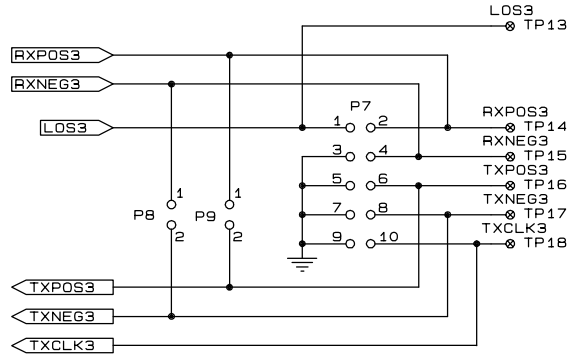
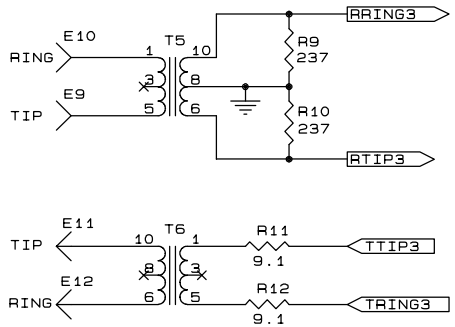


CHANNEL 1

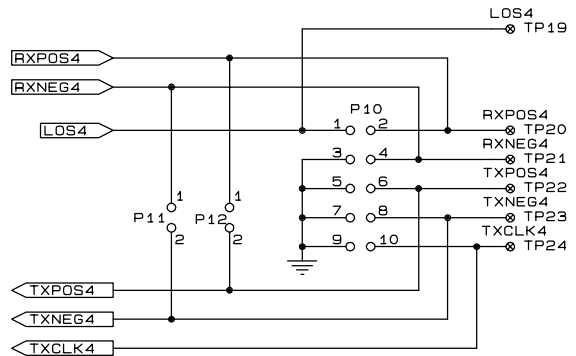
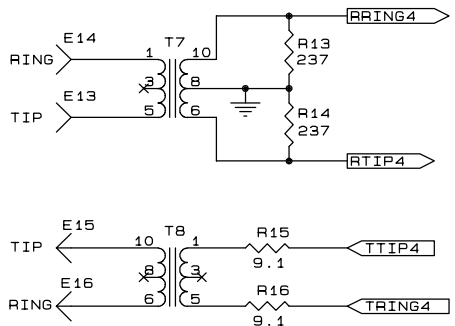


CHANNEL 2

Figure 2b. XRT5897 Demo Board Circuit Diagram

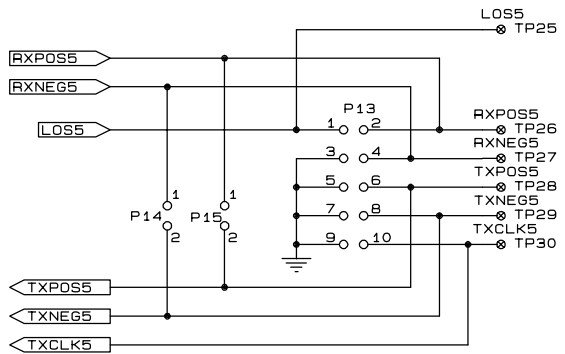
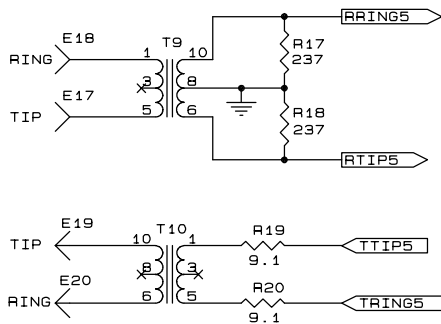


CHANNEL 3

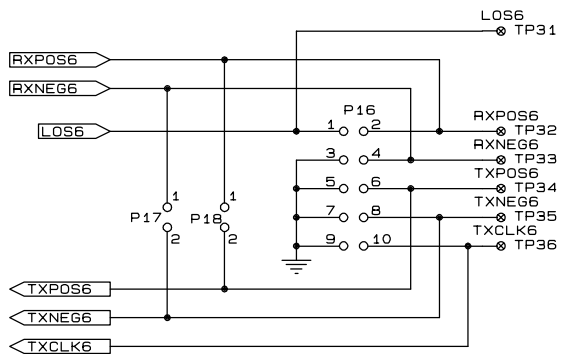
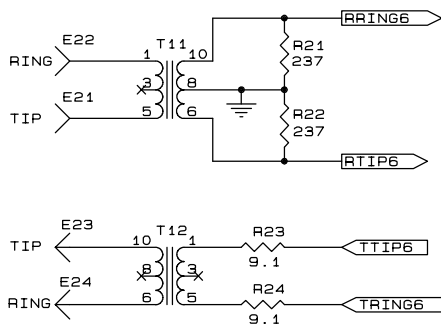


CHANNEL 4

Figure 2c. XRT5897 Demo Board Circuit Diagram



CHANNEL 5



CHANNEL 6

Figure 2d. XRT5897 Demo Board Circuit Diagram

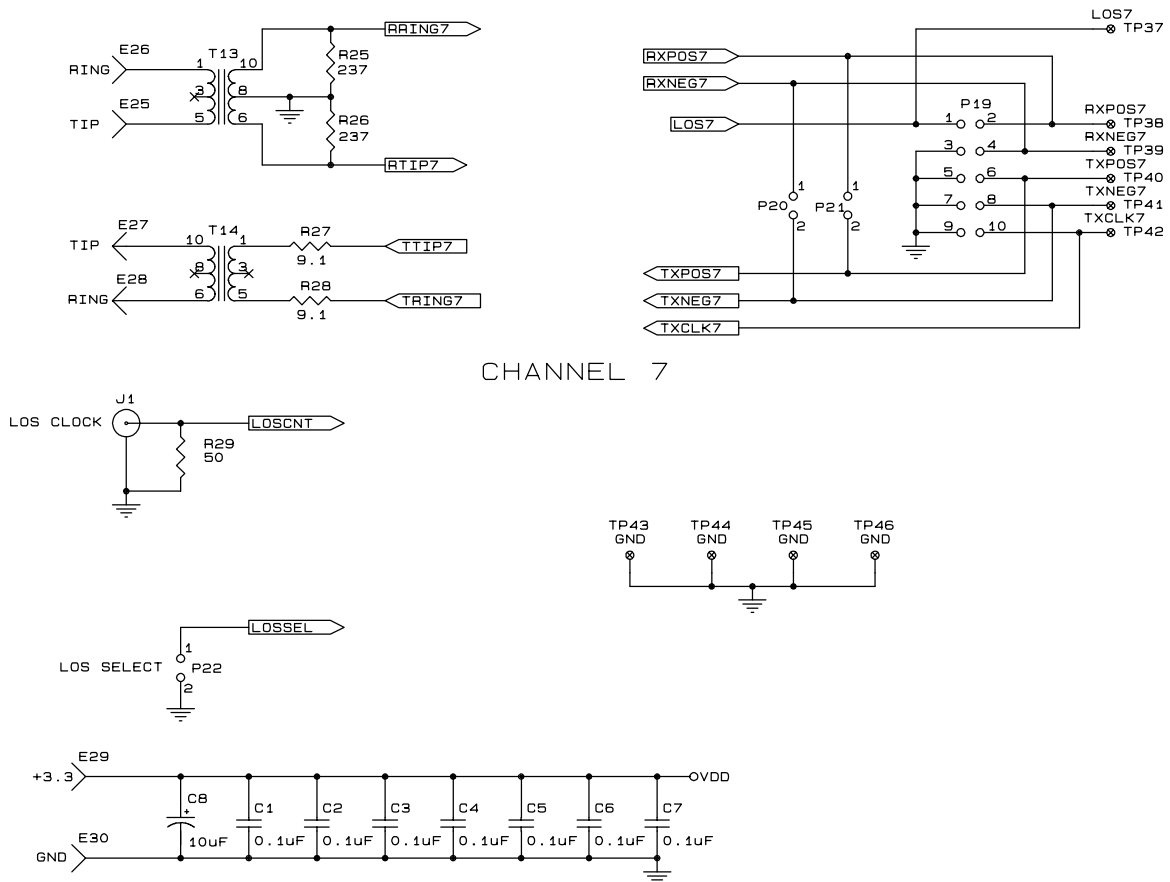


Figure 2e. XRT5897 Demo Board Circuit Diagram

Qty	Reference	Description	Supplier
14	T1,2,3,4,5,6,7,8,9,10, 11,12,13,14	Transformer, 1CT:2CT Ratio	Pulse Corp. PE-65835
14	R1,2,5,6,9,10,13,14, 17,18,21,22,25,26	237 W, 1/4 W, 1% Metal Film Resistor	
14	R3,4,7,8,11,12,15,16,19, 20,23,24,27,28	9.1 W, 1/4 W, 1% Metal Film Resistor	
1	R29 Film Resistor	50 W, 1/4 W, 1% Metal	
7	C1,2,3,4,5,6,7	0.1 mF, 63 V, Z5U Dielectric, Axial lead, 0.1" Spacing	
1	C8	10 mF, 16 V, Electrolytic, Axial lead, 5mm Dia., 2mm Spacing	
1	J1 Connector	PC board mount BNC	
14	(Connectors for Balanced Line)	3-Conductor 1/4" Audio Jack, for 3/8" hole	Switchcraft
15	P2,3,5,6,8,9,11,12, 14,15,17,18,20,21,22	2-pin header, gold	
15		Shorting jumper for 2-pin header	
7	P1,4,7,10,13,16,17	10 pin dual-row header, gold	
46		Pins for Test Point connections	
2		Banana Jacks (1 Black and 1 Red)	GND, +3.3V
4		Spacers to elevate board	
4		4-40 x 5/16" screws for spacers	
1		Test Socket for 100 pin SQFP package	Nepenthe - QPI-100050***

Table 2. XRT5897 Demo Board Parts List

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